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ABSTRACT

An address pattern generator for generating regular addresses in ~~circuits~~ a freely set inside area of the memory cell to be tested. The arrangement of the column address generator is structured the same as that of the row address generator wherein both the column address generator and the row address generator receive an add signal from a control circuit, address values from first and second maximum value registers and address values from first and second initial value registers. The column address generator has a comparator which compares an address to be supplied to the memory to be tested with the address value output from the first maximum value register and a selection circuit which selects address to be supplied to the memory using a signal output from the comparator.